#1. (30 points, 2 points each) Circle T for "true" or F for "false."

* A page fault always leads to a program crash.  
   **F**

* With hardware support, it is possible for guest virtual machines to directly interact with DMA devices in a secure, efficient manner.  
   **T**

* The Global Offset Table is used for vectored interrupts in the kernel.  
   **F**

* A processor memory bus is typically synchronous because of the need for high bandwidth.  
   **T**
* Asynchronous buses require handshaking protocols.

T

* An I/O bus is typically synchronous because the bus needs to be long and fast, and synchronous buses do not have clock skew.

F

* When you compile a typical “hello world” program in GNU/Linux, the compiler must know the exact location where the printf function will be mapped in the libc library so that it can statically bind the function pointer that your main program calls.

F

* The miss rate of a cache is equal to 1 minus the hit rate.

T

* A small victim cache can help to reduce conflict misses without requiring an increase in the associativity of a cache.

T

* DMA allows the CPU to do useful work instead of spending time doing data transfers to/from I/O devices.

T

* C compilers always use the signed integer instructions on MIPS machines so that the programmer doesn't need to think about integer overflows while writing a program.

F

* Polling is an I/O scheme that employs interrupts to indicate to the processor that an I/O device needs attention.

F
* RAID negates the need for backups, since if you accidentally delete a file it can be reconstructed by the RAID controller.

F

* Memory-mapped I/O is slowly replacing DMA because of its performance benefits over DMA.

F

* Virtual machines are a relatively new idea that was invented by the VMWare company.

F

#2. (12 points, 3 points each) For each pair of devices listed, circle the one of each pair that would be most likely to connect to the processor-memory bus (north bridge) instead of the I/O bus (south bridge).

10 Gbit Ethernet vs. 100 Mbit Ethernet

High-end graphics card vs. Large-capacity hard drive

DRAM vs. USB 2.0

south bridge vs. mouse
#3 (15 points, 3 points each).

RAID 0 – Striped
RAID 1 – Mirrored
RAID 3 – Bit-interleaved parity
RAID 4 – Block-interleaved parity
RAID 5 – Distributed block-interleaved parity
RAID 6 – P + Q redundancy

Match each improvement in performance and/or reliability with the step up in RAID that it is associated with by writing the correct character on the line. The character “d” is placed for you as an example, and there should be a one-to-one mapping.

a. By putting parity blocks on all disks instead of just one, some small writes can be performed in parallel.
b. By adding redundancy, it is possible to handle a single self-identifying failure.
c. By adding a second check, two failures can be handled.
d. By accessing data differently, small reads and writes can be done without accessing all disks.
e. By using parity, it is possible to reduce the storage overhead of redundancy from 100% overhead to 1/N where N is the size of a protection group.

RAID 0 to RAID 1: ___b___

RAID 1 to RAID 3: ___e___

RAID 3 to RAID 4: ___d___

RAID 4 to RAID 5: ___a___

RAID 5 to RAID 6: ___c___
#4. (35 points, 5 points each) Multiple Choice (circle all that apply):

* Which of these aspects of a computer architecture can affect the performance and design of virtual machines based on that architecture?:

   a. The Instruction Set Architecture (ISA)
   b. The design of the I/O system
   c. The exact semantics of privileged instructions
   d. The design of the virtual memory system
   e. The design of the DMA system

* Possible solutions to cache coherency problem for DMA include (but are not limited to):

   a. Use existing cache coherency protocols like MESI
   b. Make the on-chip cache write-back instead of write-through
   c. Route DMA reads and write through the cache
   d. Mechanisms for the OS to invalidate/flush cache lines
   e. Require all DMA accesses to be for contiguous physical memory

* Possible solutions to virtual vs. physical address problem for DMA include (but are not limited to):

   a. Use existing cache coherency protocols like MESI
   b. Make the on-chip cache write-back instead of write-through
   c. Route DMA reads and write through the cache
   d. Mechanisms for the OS to invalidate/flush cache lines
   e. Require all DMA accesses to be for contiguous physical memory
* Which of these is likely to happen if I increase associativity in a cache, but hold all else (total size, cache line size, etc.) the same:

a. The number of capacity misses will go down.

b. **The number of conflict misses will go down.**

c. The number of compulsory misses will go down

d. **The hit time will go up.**

e. The miss penalty for misses in that cache will go down.

* Which of these might happen if I increase the cache line size (or block size) in a cache, but hold all else (total size, associativity, etc.) the same:

a. **The miss rate for that cache might go up.**

b. **The miss rate for that cache might go down.**

c. **The number of conflict misses in that cache might increase.**

d. I might be able to take advantage of more spatial locality.

e. I might reduce the miss penalty for misses to that cache.

* Which of these is likely to happen if I increase the total size of a cache, but hold all else (associativity, cache line size, etc.) the same:

a. **The number of capacity misses will go down.**

b. **The number of conflict misses will go down.**

c. The number of compulsory misses will go down

d. **The hit time will go up.**

e. The miss penalty for misses in that cache will go down.
Which of the following measurement scenarios are possible:

a. A *superscalar processor has IPC > 1.0.*

b. A scalar pipelined processor with forwarding support has IPC > 1.0.

c. A scalar pipelined processor without forwarding support has IPC > 1.0.

d. A *superscalar processor has IPC < 1.0.*

e. A scalar pipeline has CPI < 1.0.


*David Patterson.*

#6 (1 point) What security model was the VAX Virtual Machine Monitor targeted at?

*Multi-level security.*

#7 (3 points) How many sets does a fully set-associative cache have?

*One.*

#8 (2 points) How many cache lines per set are there for a direct-mapped cache?

*One.*

#9 (1 point) In the movie, *Tron*, what is the name of the program that is the main villain of the film? Hint: it's three words.

*Master Control Program*