

CS341I Fall 2009 Test #2

Friday, 9 October 2009 10-10:50am

Name: Key

CS 341I Fall 2009, Test #2. 100 points total, number of points each question is worth is indicated in parentheses. Answer all questions. Be as concise as possible while still answering the question. **You have 50 minutes exactly, I'll collect the tests at 10:50am.** Closed book, closed notes, closed calculator, closed everything. If a question is ambiguous, state your assumptions before answering it.

#1. (28 points, 2 points each) Circle T for true or F for false.

* Pipelining increases instruction throughput, it typically does not decrease instruction latency.

T

* An instruction placed in a branch delay slot is always executed, whether the branch is taken or not.

T

* A branch target buffer and a branch predictor are the same thing, just two different names.

F

* Tomasulo's algorithm performs a dynamic form of register renaming.

T

* Precise interrupts are no longer important because modern processors have superscalar pipelines.

F

* In floating point numbers, I can always assume that $(a + b) + c = a + (b + c)$, but not necessarily that " $a + b = a$ " is not true when b does not equal 0.

F

* J-type instructions such as `jal` and `j` use pseudo-direct addressing. T

* Pseudo-direct addressing can reference any byte in a 32-bit address space using only the bits that are encoded in the J-type instruction.

F

* MIPS is no longer commonly used because it is a Complex Instruction Set Computer (CISC) processor.

F

* Load and store instructions in MIPS (`lw`, `sw`, etc.) use PC-relative addressing.

F

* Conditional branch instructions in MIPS (`beq` and `bne`) use base+offset addressing where the base is loaded from a general purpose register and the offset has a range of about -2^{15} to 2^{15} bytes.

F

* A scalar pipeline such as MIPS enables us to achieve $IPC > 1.0$.

F

* A "petaflop" supercomputer will always run any possible program you could give it faster than a "900 teraflop" supercomputer would.

F

* A correlating branch predictor combines local branch behavior with global information about the behavior of some recent branches, for increased accuracy.

T

#2 (10 points) Of the two semantically equivalent sequences of MIPS code below, which will have the fewest number of bubbles when executed in a typical MIPS pipeline as in Chapter 4 of the book? Another way to phrase this question is: which sequence would a smart compiler be most likely to produce?

a. A

b. B

#3 (10 points) Of the same two semantically equivalent sequence of MIPS code, which requires the most forwarding of data to occur?

a. A

b. B

A.		B.	
lb	t0, 0(s1)	lb	t0, 0(s1)
addi	t0, t0, 48	lb	t1, 1(s1)
sb	t0, 0(s2)	lb	t2, 2(s1)
lb	t0, 1(s1)	lb	t3, 3(s1)
addi	t0, t0, 48	addi	t0, t0, 48
sb	t0, 1(s2)	addi	t1, t1, 48
lb	t0, 2(s1)	addi	t2, t2, 48
addi	t0, t0, 48	addi	t3, t3, 48
sb	t0, 2(s2)	sb	t0, 0(s2)
lb	t0, 3(s1)	sb	t1, 1(s2)
addi	t0, t0, 48	sb	t2, 2(s2)
sb	t0, 3(s2)	sb	t3, 3(s2)

#4 (24 points, 6 points each) Multiple choice. Circle the one correct answer.

*Which of the following things would you most typically do to address a structural hazard?

a. **Build a separate adder, in addition to the ALU, for program counter calculations**

b. Do data forwarding

c. Add a branch delay slot to your ISA

d. Branch prediction

*Which of the following things would you most typically do to address a control hazard?

a. Build a separate adder, in addition to the ALU, for program counter calculations

b. Do data forwarding

c. Multi-port the register file

d. **Branch prediction**

*Which of the following things would you most typically do to address a data hazard?

a. Build a separate adder, in addition to the ALU, for program counter calculations

b. **Do data forwarding**

c. Add a branch delay slot to your ISA

d. Add a branch target buffer

* What typically happens if a branch is mispredicted?

* We have to insert a bubble to delay the next instruction

* **We have to flush the pipeline**

* We throw an exception and the operating system kills the process

* The program gives incorrect results.

#5 (10 points) Use the following equation for Amdahl's law to answer the question:

$$O.S. = 1/((1-f)+(f/s))$$

Suppose you're building an embedded processor to compete with the ARM/XScale ISA, and using a MediaBench benchmark. You need to shave 20% off of your total execution time for that particular benchmark. You think you can increase the performance of memory copy loops by a factor of 5 by increasing the cache bandwidth. What fraction of the total execution time of the benchmark would need to be currently being spent on memory copy loops in order for this optimization to achieve your target for the overall speedup?

Plug in $s = 5$ and $O.S. = \text{Exec. time old}/\text{Exec. time new} = 1/0.8 = 1.25$

Solve to get $f = 0.25$

#6 (10 points) Use the following equation for Amdahl's law to answer the question:

$$\text{O.S.} = 1 / ((1-f) + (f/s))$$

Suppose 8/9ths (or 0.888888...) of the serial execution time of my scientific computation is trivially parallelizable, meaning that I can take that 8/9ths of the work and divide it up among N nodes on a N-node cluster and that part of the execution will run N times as fast. How many nodes in my mini-cluster would I need to get an overall speedup of a factor of 5?

Plug in $f = 8/9$ and O.S. = 5, solve to get $s = 10$

#7 (5 points) Why is a superscalar processor (*e.g.*, one that uses Tomasulo's algorithm) able to achieve $IPC > 1.0$ and get better performance than a scalar pipeline?

Instruction Level Parallelism (ILP)

#8 (1 point) What machine was Robert Tomasulo designing a floating point pipeline for when he came up with Tomasulo's algorithm?

IBM System/360 Model 90

#9 (1 point) In what year did Robert Tomasulo win the Eckert-Mauchly award?

1997

#10 (1 point) Name a DSP chip where the hardware will not resolve data hazards for you by inserting bubbles, and you may get incorrect results for your computations if you're not careful.

TI TMS320C6000

#11 (no points) In terms of fried eggs (not hard boiled), what is the opposite of "over easy"?

I still don't know the answer to this :-)

#12 (no points) In the *Texas Chainsaw Massacre*, the hitchhiker describes a type of "cheese" to the travelers in the beginning of the movie when they give him a ride in their van. What type of "cheese" was he describing?

Head cheese