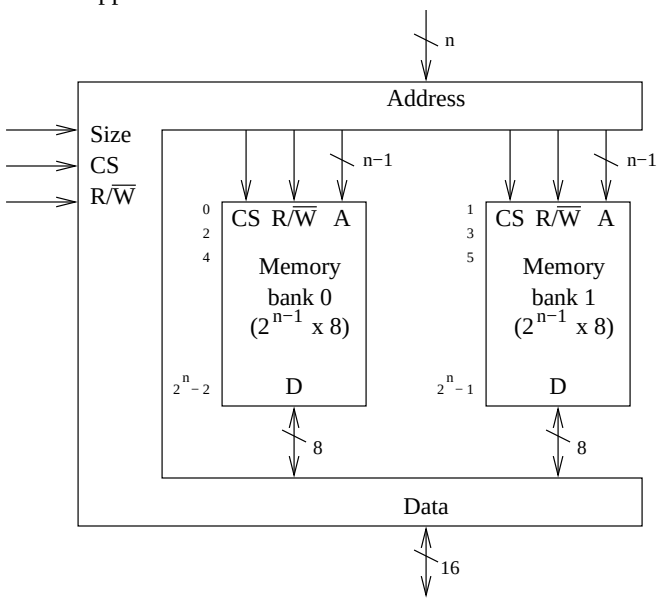
1. Consider the details of the following organization. As we have noted, this organization can support access to 8-bit and 16-bit values.

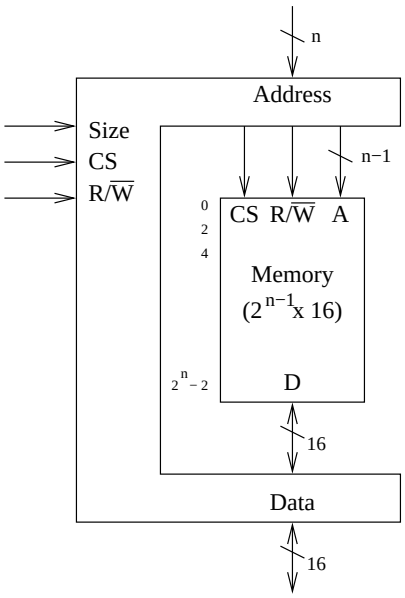


Assume that a 0 on the Size signal is used to indicate a byte operation.

a. Design a circuit that routes the address, CS, and R/$\overline{W}$ to the internal memory banks of the memory system. Do **not** assume that 16-bit accesses must be aligned.

b. Assuming that the data port is justified, design a circuit that routes the data inputs/outputs of the memory banks to the correct lines of the data port. (Assume that the memory is 4 bits wide and that each bank is 2 bits wide.)

2. Consider the details of the following organization. Like the previous organization, this organization can support access to 8-bit and 16-bit values.



Assume that a 0 on the Size line is used to indicate a byte operation and that 16-bit memory accesses must be aligned.

a. Design a circuit that will correctly route the data output signals from the internal memory assuming that the data port is justified.

b. This organization is inefficient when you need to store a single byte. It is difficult to make sure that you only write over the correct byte of the memory word. One solution is to use two steps whenever you need to write a single byte. During the first step the current value of the appropriate word is read and stored in a register. During the second step, the value in the register is combined with the input byte and written back to the memory. Design a sequential circuit that implements this solution. In designing this circuit, assume that the two clock signals (step 1 and step 2) are provided.

3. In this exercise we consider the relation between cache hit rate and effective access time for a variety of cache access times. We limit our consideration to a memory system that uses a one level cache and a main memory access time of 50 nanoseconds.

   For the cache access times listed below, prepare a graph that relates effective access time to cache hit rate. The horizontal axis of your graph should be labeled with the hit rate and the vertical axis should be labeled with the effective access time. You should calculate the effective access time for hit rates of 0%, 10%, 20%, etc.

   a. 5 nanoseconds

   b. 10 nanoseconds

   c. 15 nanoseconds

d. 20 nanoseconds

e. 25 nanoseconds

4. For each of the following C statements, give a sequence of instructions, from those described our simple accumulator machine that will evaluate the statement. In writing the code sequences, assume that the values for *a*, *b*, *c*, *d*, and *e* are stored in memory locations 20, 21, 22, 23, and 24, respectively. In addition, you may assume that memory locations 28, 29, 30, and 31 can be used to store intermediate results as needed. (Note: % is the **mod** operator of C.)

   a. e = a + b $*$ d;

   b. e = a $-$ b $*$ c;

5. Translate each sequence of instructions from the previous exercise into the machine language for our simple accumulator machine.

6. Explain how you would generate the control signals needed to control the function of the ALU (i.e., control points 10 and 11).

7. Our implementation of the CPU for the accumulator machine does not provide any means to alter the value of the program counter (PC) other than the increment in the ifetch loop. Suppose that the OPCODE 110 is used to set the PC to the value stored in the address field of the instruction.

   a. Describe how you would alter the flowchart shown in Figure 3.13 to accommodate this new instruction.

   b. Explain how your changes impact the next-state logic. Give circuits that illustrate changes in the generation of the next state.

8. Search the Internet and find prices for RAM. What are the general factors that affect price (e.g., size and speed)? Explain how these factors are related and tie tour discussion to specific examples.

Thu, 16 Oct 1997 09:41:59 -0600