Chapter 11
Buses and I/O Devices

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Overview

- Synchronous protocols
  - synchronous protocols use a clock
  - asynchronous protocols don't have a clock
    * typically, faster (no waiting for the clock to strike)
    * typically more complicated
- Timing considerations
- Arbitration

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Bus Signals

Line/signal	Established by
Start	Initiator (Master)
Data	Initiator/responder (Master/slave)
Address	Initiator (Master)
$R/\overline{W}$	Initiator (Master)
Done	Responder (Slave)
Clock	Bus

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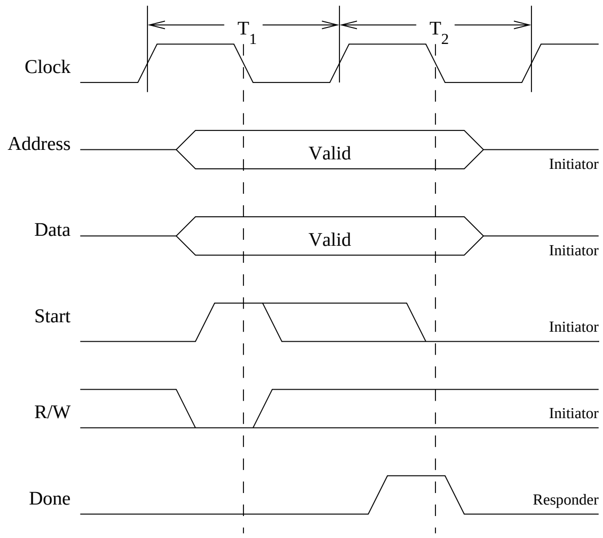
Timing for a Write Transaction



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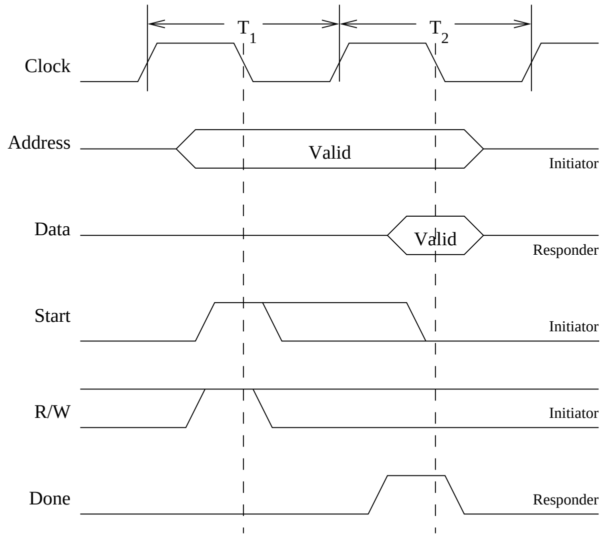
Timing for a Read Transaction



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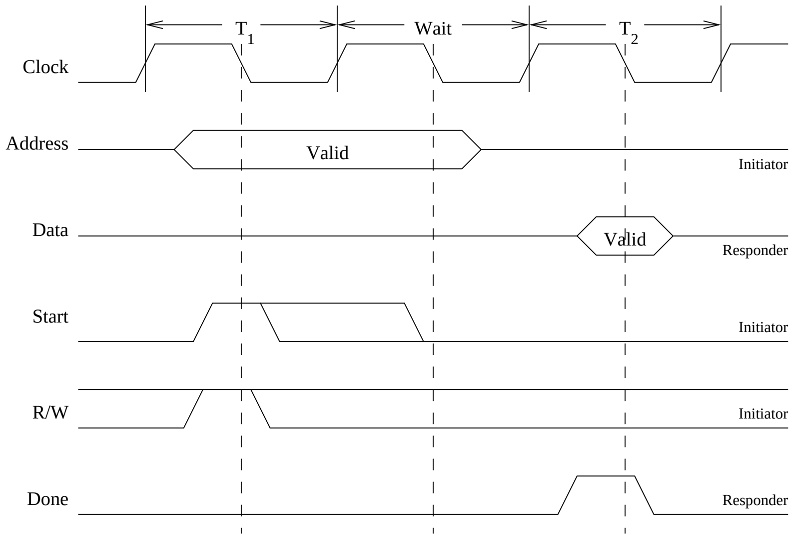
Wait States



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Timing Considerations

1. *Transaction access time*: from when **responder** recognizes **start** signal until **responder** asserts **done** signal
2. *Transaction cycle time*: interval between consecutive requests
3. Calculating wait states

a	access time
s	bus stabilization time
b	bus clock cycle time
w	number of wait states

$$a \leq 1.5 \cdot b + w \cdot b - 3 \cdot s$$

$$w \geq \frac{a - 1.5 \cdot b + 3 \cdot s}{b}$$

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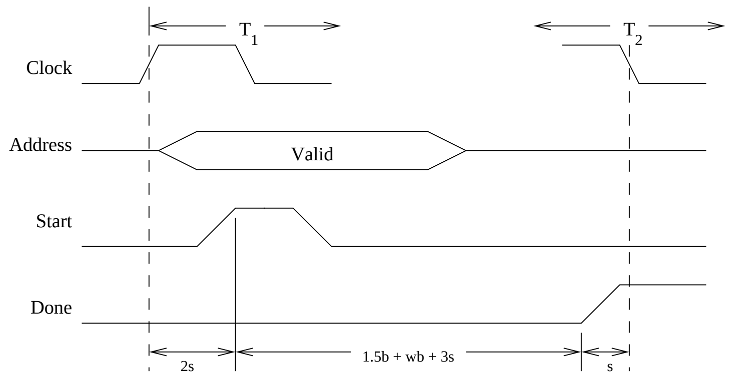
Bus Timing



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Example 1

- Assumptions
  - bus clock 16.67 MHz
  - bus stabilization time is 10 nanoseconds
  - access time is 80 nanoseconds
- Bus cycle time

$$\frac{1}{16,670,000}\frac{\text{sec}}{\text{cycle}} = \frac{1,000,000,000}{16,670,000}\frac{\text{nanosec}}{\text{cycle}} \approx 60\frac{\text{nanosec}}{\text{cycle}}$$

- Number of wait states

$$\begin{aligned} w &\geq \frac{80 - 1.5 \cdot 60 + 30}{60} = \frac{20}{60} \\ \Rightarrow w &= 1 \end{aligned}$$

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Example 2

- Assumptions
  - bus clock 12.5 MHz (80 nanosecond cycle time)
  - bus stabilization time is 10 nanoseconds
  - access time is 80 nanoseconds
- Number of wait states

$$\begin{aligned} w &\geq \frac{80 - 1.5 \cdot 80 + 30}{80} = \frac{-10}{80} \\ \Rightarrow w &= 0 \end{aligned}$$

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The Effect of Cycle Time

- Access time identifies the *minimum* number of wait states
- Assumptions
  - bus stabilization time, 10 nanoseconds
  - 25 MHz clock (40 nanoseconds)
  - access time (read or write) is 20 nanoseconds
  - write cycle time is 160 nanoseconds

$$w \geq \frac{20 - 1.5 \cdot 40 + 30}{40} = \frac{-10}{40}$$

- cycle time
  - could be as low as 80 nanoseconds (two bus cycles)
  - needs to be 160 nanoseconds, when to add wait states?